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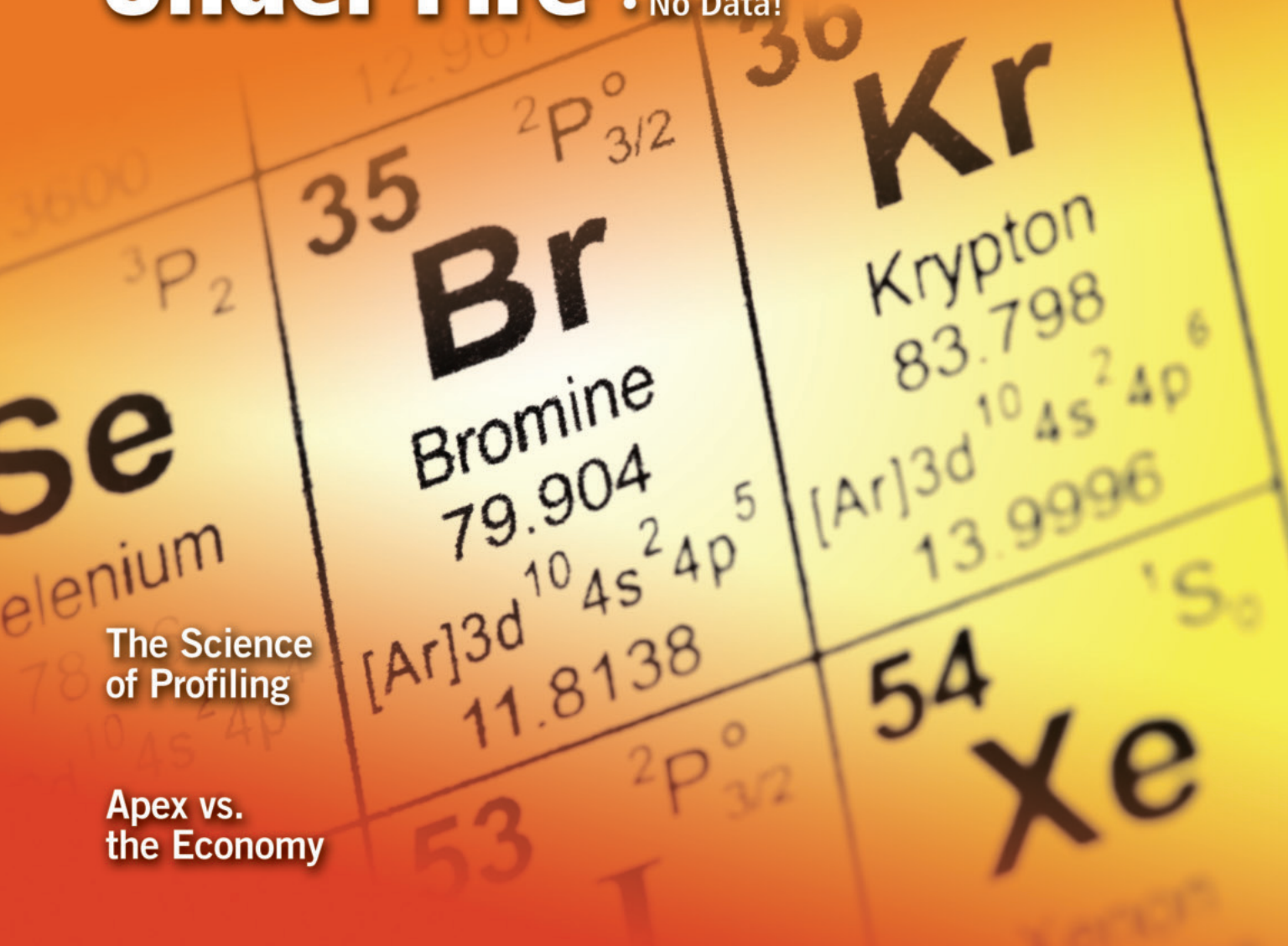
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BROMINE Under Fire

Why Defenders Argue

- Questionable Alternatives!
- No Test Methods!
- No Data!



The Science
of Profiling

Apex vs.
the Economy

SiP: Shrink Without Sacrifice

Replacing actives with bare die reduces the footprint as much as sevenfold.

As electronics technology progresses, system miniaturization drives more function into smaller and lighter packages, increasing package density. The tighter line widths and spaces and smaller vias required by the increase in density are ideal for high wireability packaging solutions. In applications where all required functions cannot be implemented on a single chip, using system-in-package (SiP) best answers the miniaturization need without sacrificing performance.

Traditional system assemblies consist of a printed circuit board with numerous packaged modules, components and connectors for communicating outside and within the system. All these electronic devices and components communicate through the board, integrating a variety of functions. Redesigning these devices and component assemblies into a SiP significantly reduces the number of components necessary for the system to function. By replacing the packaged components with bare die, sweeping the passives off the board surface, migrating to fine-pitch connectors and incorporating high-density interconnects, the size, height and weight of the product can be significantly reduced.

SiP uses bare die to get a lot of function in a small space. Replacing active packages with bare die reduces the required footprint for that particular function as much as sevenfold, and significantly reduces pad size and pitch on the substrate necessary to accept the bare die bumps. These small, tightly spaced pads will typically require solder to be applied to the substrate before assembly to connect the flip-chip bumps on the bare die to the substrate. Using the correct amount of solder is critical: Enough solder must be applied to form a good joint, but too much solder will bridge the joints during soldering. However, this approach drives a very dense and advanced substrate design, fabrication and assembly. Analog, digital, and memory flip-chip devices are mounted on the SiP using advanced substrate methods.

On traditional assemblies, capacitors, resistors and inductors usually dominate the board surface. Embedding capacitance material into the structure of the substrate minimizes the requirement for a number of these components, but also increases fabrication complexity and material costs of the substrate. Applying thin-film resistor materials to copper foils or screening resistor materials enables the resistor technology to be embedded into the SiP substrate. These materials can then be trimmed to the required value using a laser.

To optimize functionality, the large connectors are

replaced with fine-pitch connectors. Replacing large, bulky connectors with patterning interconnects that have fine-pitch edge mounted units greatly reduces substrate size. This technique also optimizes the functional area of the package where most of the critical system communication is required. A single 1 mm space connector can reduce the connector(s) footprint by 5X, but will result in higher wiring demands of the substrate to enable in-and-out wiring of the perimeter-mounted substrate.

The substrate must be able to support HDI, which is essential to minimizing size and weight and maximizing performance. An advanced SiP requires high wireability, not only in the x-and y-directions with small circuit lines and tight spacing, but also in the z-direction to accommodate communication between tightly spaced components on both the top and bottom of the substrate. To provide an order of magnitude, this means a substrate at least 25 μm circuitry traces, 50 μm diameter microvias, and 5 μm diameter plated through-holes. The increased interconnect density increases the number of components placed in a given area. HDI is the best method for evenly and effectively balancing the SiP design with component placements on both sides of the substrate.

To provide a smaller package with increased performance and usability, an effective SiP requires a combination of advanced substrate features and component miniaturizations, all of which interact to achieve the desired package function and performance requirements. Active devices and components must be removed from their traditionally large packages and assembled directly onto a substrate designed to accept direct chip attach. Embedded passive layers and components must replace the traditional surface mounted components to free critical substrate space, which in many cases will improve the electrical performance of the package. Communication off the substrate must be consolidated and minimized with new connector solutions, and the placement of all these devices and components will be critical to overall package size reduction and performance. These requirements drive dense component placement and demand dense routing requirements of the substrate. The substrates necessary for a SiP with bare die can be more costly, and the fabrication and design more complex, but the benefits of a smaller, lighter, and higher-performing product usually outweigh the development difficulties. ■

Ed.: We welcome Jeff Knight to our lineup of columnists. His column will run bimonthly.

Jeff Knight is vice president of business development at Endicott Interconnect Technologies (eitny.com).

