PACKAGING HIGH DENSITY CAPACITIVE MICRO-MACHINED ULTRASONIC TRANSDUCERS (cMUT) SENSOR ARRAYS USING HYPERBGA® TECHNOLOGY

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ABSTRACT

Piezoelectric transducers have long dominated ultrasonic transducer technology, but capacitive micro-machined ultrasound transducers (cMUTs) have emerged as an alternative. Features of cMUT devices are wide bandwidth, ability to use MEMs (Micro Electro-Mechanical Systems) silicon fabrication methods to produce large arrays and potential for integration with supporting electronic circuits. cMUT technology can potentially produce the type of integrated sensor array to enable advanced 3-D imaging. A major challenge to achieve this goal is how to package these cMUT devices such that one can produce a large sensor array for imaging. We have used a high density Teflon interposer called HyperBGA® technology, produced by Endicott Interconnect to design a modular package in which the sensor cMUT array is on the topside and the supporting electronics on the backside. The cMUT devices are flip chip attached to the interposer and are spaced 100um between adjacent die. A 40 mm module size was built having a 4x12 array of cMUT devices in the center region of the module that are flip chip attach to the topside of the interposer. Each cMUT device is 3 mm in size with an element pitch of 185 um and having a 16x16 element array. On the backside are three 10mm x 11mm ASIC die having a pad pitch of 150um, each die having about 4100 I/O pads. In addition, there are about 648 BGA pads with a 1.0 mm pitch on the backside for attach to a 2.85 mm board. The packaging challenges to design and build this type of advanced sensor array will be presented.

Key words: HyperBGA® interposer, trenched cMUT device, modular package, tiled array, PTFE-based interposers.

INTRODUCTION

In this work two types of cMUT sensor packages were designed: First a functional module was designed and built to test the cMUT devices. For this design, a 42mm HyperBGA® interposer was used that accommodated a 4x12 array of cMUT devices in the center of the module. On the backside of this functional cMUT device module, 3 mechanical ASIC chips were attached to simulate the stresses generated in the next generation of package along 648 1.0 mm pitch BGA pads. In the second design, which we refer to as the “Packaging Test Vehicle” a full array of cMUT sensors are brick walled on the top of the substrate and supporting electronics are attached on the backside of the module. There will also be 0.5mm pitch BGA pads on the backside of this module to allow for assembly to the next level. This module can then be tiled onto a board to create a larger sensor array.

In the functional module (referred to as the 1A design) there is a 4 x 12 array of die closely spaced on an organic substrate to create a 12mm x 36mm cMUT transducer probe. The main purpose of this package was to be able to fully test the functionality of a larger cMUT sensor array for various medical applications. The schematic layout for front view of this module is shown in Figure 1. Essentially the functional cMUT region covers an area of about 6mm x 36mm. Only the two internal rows are functional cMUT devices, the two outer rows are dummy cMUT die. A cross-sectional view of this module is shown in Figure 2. Here dummy ASIC devices are flip chip attached on the backside. There are 3 locations under the 4x12 cMUT array for the dummy ASIC die to be attached. Each die has ~4100 I/O pads with a pitch down to 150um. Both eutectic Sn-Pb and Pb-rich solder bumps were evaluated. The 1.0 mm pitch BGA pads use a eutectic Sn-Pb solder alloy. The module is attached to a PWB using a standard BGA no clean solder attach process. As a result of the sensitivity of the cMUT device, we do no wish to expose these devices to a water clean operation to remove any water-soluble flux residue.

In the second package design, a single module that could be tiled to create a larger sensor array was envisaged. If one of the modules became bad, the module could be removed and a new one put in its place, offering the feature of reworkability. Ultimately we would like to create a module having on the topside a full array of closely spaced cMUT die and on the backside the support electronics using ball grid array (BGA) solder interconnections to connect to the next level of carrier. In order to show the feasibility of this type of design we plan to design a packaging test vehicle to show the viability of a high-density array of cMUT die spaced at 100um apart. One should note that this is the spacing of cMUT die used for the functional design. Once we have shown that this type of package can be built and passes the specified reliability requirements, we will then proceed to build the functional module. This second type of test vehicle is what we call the modular packaging test vehicle (referred to as the 1C design). Ultimately, this would be the building block to create not only cMUT sensor arrays, but also a generic packaging solution for any type of sensor array with the backside support electronics. Figure 3 shows an illustration of a cross section of the module attached to the board and a top view.

For both of these packages, a cMUT sensor die having a backside trench was used. The details of solder bumping these types of die were the topic of the other paper reported at this conference entitled: Challenges of solder bumping capacitive micro-machined ultrasonic transducers (cMUT) trenched devices [1].” This feature creates tremendous packaging challenges, not only for bumping a trenched wafer, but the challenges with first level interconnect reliability without an underfill. This is mainly driven by the need to create a near seamless cMUT cell sensor array, which requires the die to be closely spaced. The first goal of this work as previously mentioned was to package die with 100um spacing, however, performance requirements will need this space to go down to 50um and less. In addition, the flatness of module needs to be within 610um, which will greatly increase the challenges of packaging. A schematic illustration of the trenched cMUT device is shown in Figure 4.

HyperBGA® is a high performance and high reliability PTFE-based (Teflon) chip carrier technology manufactured by Endicott Interconnect Technologies (EI), Endicott, NY [2]. PTFE provides a low dielectric constant ($\varepsilon r = 2.7$) and low dielectric loss ($\tan \delta = 0.003$), which translates to superior electrical performance. A standard HyperBGA® is composed of 9 low loss copper metallization layers. Specifically, the laminate contains two signal layers utilized for a majority of the signal routing, Signal 1 and Signal 2. Both of these layers are completely embedded in a true stripline environment (sandwiched between either Voltage 1 or Voltage 2 and the center copper-invar-copper (CIC) ground plane). In addition to the signal routing layers, are two redistribution signal layers, top surface redistribution (TSR) and bottom surface redistribution (BSR). The redistribution layers are designed to establish wiring channels, which allow the signal routing layers to efficiently match the C4 footprint to the desired BGA footprint. The C4 layer on the very top of the substrate contains only the C4 pads while the BGA layer on the very bottom of the laminate contains only the BGA pads. Interlayer connections are accomplished with microvias and plated through-holes (PTHs).

RESULTS

The substrates used for this evaluation were made using EI’s HyperBGA® packaging technology. For the 1A functional design EI will use their existing 9-layer HyperBGA® substrate. For the 1C design an 11-layer cross-section will be necessary. This 11-layer substrate is a modification enhancement to the existing 9-layered cross-section.

Substrate 1A NIP Design

In order to be able to show that one can successfully attach a trenched cMUT device to a HyperBGA® substrate, a no-internal-planes (NIP) test substrate was built. Dummy trenched cMUT devices were assembled on the topside of the interposer along with backside ASICs to show that one can successfully assembly such a package cross-section and maintain a relatively flat interposer. Figure 5 shows a photograph of the first NIP assembly. In this package design eutectic Sn-Pb solder was used for the trenched cMUT devices and the backside dummy ASICs. This assembly did not use a thinned ASIC die, which is unacceptable for future packaging evaluations, since the BGA balls cannot be attached to board. The actual 1A functional design requires a 100um thinned mechanical ASIC die, which will then allow for complete BGA attach to the board. The main purpose of this work was to show that the topside cMUT devices and the backside ASICs can be attached to a HyperBGA® interposer and remain flat.

Substrate 1A Functional Design

A functional HyperBGA® substrate and associated board was designed and built at EI. The HyperBGA substrate was a standard 9-layer x-section, which represents what is in production today. Functional cMUTs were bumped with eutectic Sn-Pb solder and diced. In addition, dummy ASICS were flip chip attached on the backside along with the placement BGA balls. The assembled substrate will be attached to an imaging board. This completed unit will then be tested at GE to ensure complete functionality. A goal of this project is to produce a small quantity of functional hardware for testing the cMUT devices. Since this vehicle does not use functional ASICs, a 9-layer HyperBGA® x-section can meet the design requirements for this package. These cMUT devices have a complicated trenched structure underneath the die, which makes it very difficult if not impossible to underfill. Due to the small die size and the flexibility of the HyperBGA® substrate, we think that the reliability of the trenched flip chip interconnect may be acceptable for this application. Again, future testing will be done to verify this statement.

While the substrate technology is not new, the application and functional requirements are; in particular, coplanarity is of concern for this double-sided clip chip attached module. During the design phase, there are a limited number of changes that can affect the resultant coplanarity. These include a symmetrical x-section and balancing the copper on each plane. Figure 6 schematically illustrates the ability to package the 2 rows of functional cMUTs on the HyperBGA® substrate with the adjacent dummy rows.

As this paper was being written, the initial set of 1A Functional Substrates was completed. The results of the assembly of this hardware will be presented at the conference.

Substrate 1C Packaging Test Vehicle Design

In this phase of activity a stitched laminate substrate will be designed and built at EI to simulate the actual functional interposer. Non-functional test chips, which will be stitched cMUTs and stitched ASICs have been built to simulate the actual die footprint and features. These test die will then be solder bumped. A primary goal of this phase of the project is to develop substrate technology and to successfully prototype double-sided flip chip packaging with the backside ASICs and topside cMUT test chips to the stitched substrate. The long-term goal is to achieve top surface flatness of +/- 10um of each module site after attach to the board. The 1C test vehicle is a best effort to dictate what future changes will be needed to achieve this goal. A board assembly having an array of 2x2 modules will be designed, built and tested. This test vehicle will have the feature to test the specific interconnect locations on both sides of the substrate and readout connection through the board.

The 1C module connects an 8x8 array of cMUT devices on the topside with 4 ASICS on the backside of the interposer. More than 16k nets distribute from the 150 um pitch ASICs to the 185 um pitch cMUTs and all of the nets pass through PTHs in the HypberBGA® substrate. The PTH density exceeds 35 per sq. mm and requires a 150 um PTH pitch which is an advancement over the 200 um PTH pitch available in production HyperBGA. The wiring demand required an additional 2 layers to the existing production substrate resulting in an 11-layer x-section. One might view this substrate as a high-density matrix translator. In addition, the cMUT arrays need to be placed very close to the edge of the substrate, within 100um. This is also an extension of existing technology.

Although 1C will be designed to perform as a representative functional substrate, it can also be used as a packaging test vehicle. The cMUT and ASIC test chips are designed to complete a high percentage of interconnections by probing the BGAs on the bottom of the substrate or testing through the PWB that attaches to the BGAs.

Assembly Process Development

There are multiple assembly challenges with both the 1A Imaging Vehicle and the 1C Packaging Vehicle. To assist with this effort, a NIP (No Internal Planes) vehicle was built with cMUT attachment pads on the top and ASIC attachment pads on the bottom. The advantages of a NIP are that it can be built quicker and costs less so the Assembly Development activity can start sooner using a less expensive substrate.

The coplanarity requirements for this application (+/- 10 um) will be challenging, especially since this is a double-sided C4 approach. cMUTs will be placed, without underfill on the top side, while ASICS will be placed, with underfill, on the bottom side.

As a result of the narrow 27.5um square trench that surrounds the 90um square pillar below each cMUT element, see Figure 4, that has a depth of ~250um, it is highly unlikely that one can successfully fill this trench using conventional capillary underfill dispense methods. Also, the impact of the shrinkage of the underfill after cure and the affect this may have on cMUT integrity is unknown. The cMUT devices are placed at 100um spacing from edge of die. These constraints make underfill very risky at this stage of development.

Figure 7 shows an X-ray image of the dummy trenched cMUT device attached to the NIP interposer. In this particular device 5 pillars were missing, which explains the 5 opens in this image. However, this shows very good flip chip bonding for all of the remaining bumped pillars. This same device was then shear tested to determine the failure mode. After the die was sheared, most of the failures occurred at the base of the pillar to the active cMUT device. Figure 8 shows the solder attached pillars remaining on the substrate. We know from the solder bumping work of trenched cMUT devices, that there is an under cut of the base of the trench to the cMUT that can act as a crack initiation point. This work clearly shows that these pillars are inherently weak, thus explaining why the majority of pillars fail at the base of the trench region. Future work is focused on strengthening these pillars and is the topic of the other paper presented at this conference. Figure 9 shows the failure from the trenched side of the cMUT device. Again, this reveals the effect of the under cut of the trench etching process and the impact this has on producing trenches that are weaker than expected.

DISCUSSION

The success of assembling topside cMUT devices along with a thick backside ASIC die shows that HyperBGA technology can achieve a relatively flat module as shown in Figure 5. Recent work on assembling up to 9 cMUT dummy die on the 4x12 array on the 1A functional test vehicle give us confidence that we will be successful at populating a 2x12 center area with functional cMUT die along with the two out rows with dummy cMUT die. Initial plans are to populate the 4x12 cMUT sensor array with cMUT devices without the backside dummy ASICs. Based on preliminary module builds it appears we should be able to produce modules with our target flatness of +/- 10um. This aggressive flatness is required in order to be able to successfully do ultrasound imaging.

The early cMUT designs had a die size of about 12mm for a 185um pitch and a 64x64 element array. It was difficult to achieve an acceptable die yield with this large die size and we chose to decrease the die size to accommodate a 16x16 array, which makes the die size about 3mm. Since the cMUT has a backside trench, it is difficult to underfill. By having a small distance to neutral point (DNP) along with the flexibility of the HyperBGA interposer we believe that the non-underfilled flip chip cMUT may have acceptable reliability for an ultrasound application in a hospital environment. The smaller cMUT die offers a higher yielding device along with better reliability when compared with the initial 12mm die size.

One representative cMUT was removed by pulling it with a pair of tweezers to assess (qualitatively) the joint integrity. The cMUT could not be removed using only vertical force. Only a lateral force, with a slight upward pull, removed the cMUT. This motion produced an unzipping; as the cMUT pillars broke at the base, see Figure 8. 240 pillars broke at the base out of a total of 256. The interconnect integrity appears to be quite good based on this limited data. cMUT to cMUT alignment was also very good, and no significant coplanarity issues have been noted.

Currently we are in the process of building more hardware to collect additional data. Initially cMUTs will be attached only on the top surface and we will then subject these modules to thermal cycling in order to assess the interconnect reliability. We plan to build 5 modules for this testing: One part will be sacrificed for x-sectioning immediately. 3 of the remaining parts will be subjected to thermal cycling (0-50 C) to assess how well they hold up. The shear and pull strength of the cMUT pillars will be measured to quantify the deterioration of the pillar strength with an increase in the number of thermal cycles. This information will be presented at the conference

ACKNOWLEDGEMENTS

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Figure 1: Top View of Array of 4 die by 12 die cMUT Sensor Array Module

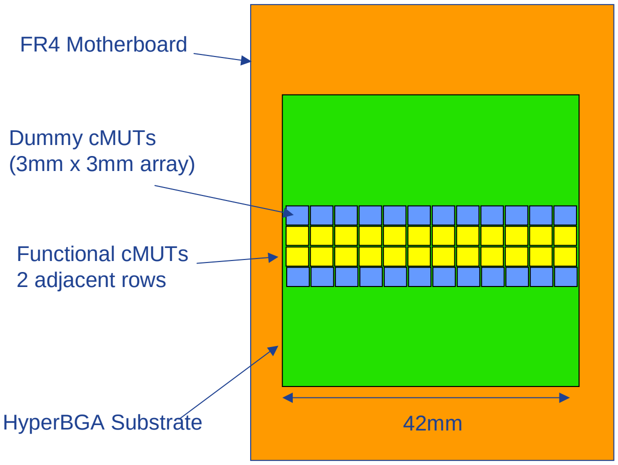
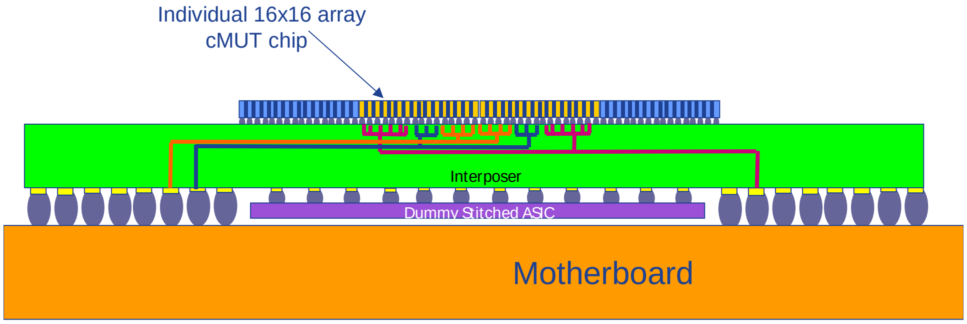


Figure 2: Cross-sectional View of Functional Module:

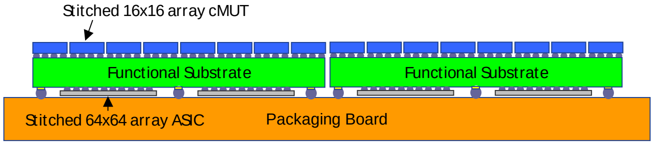
Cross-section showing *schematically* how subelements are ganged to form elements



Interposer (green) mounted to module board (orange)
using Ball Grid Array (BGA) packaging technology

Figure 3: Packaging Test Vehicle (1C Design)

Cross-section



Top View

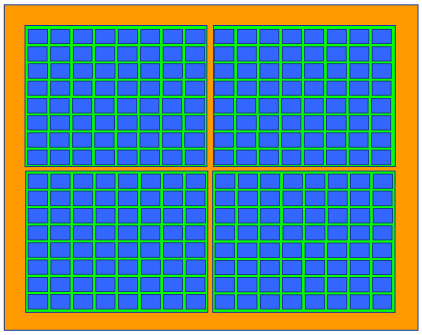


Figure 4: Cross-sectional View of cMUT

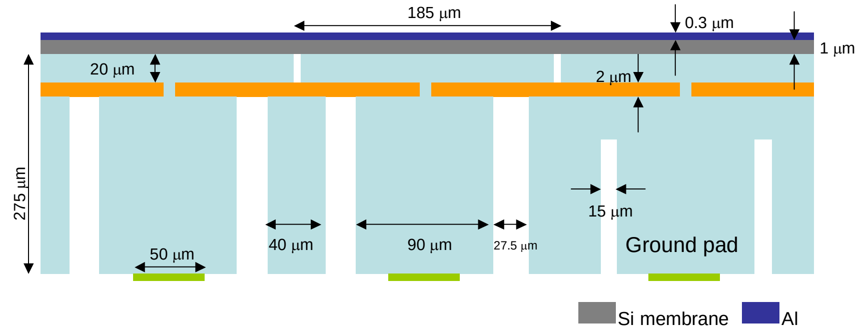


Figure 5: Feasibility Cross-Section

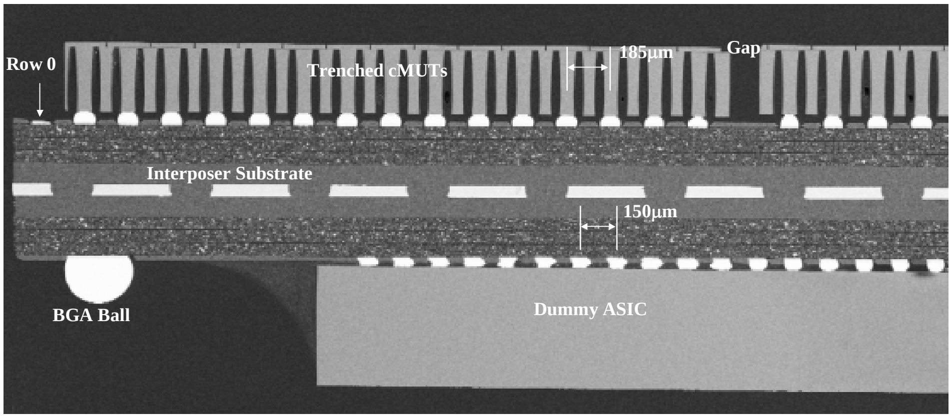


Figure 6: Cross-section of 4 adjacent cMUT devices attached on the 1A NIP test vehicle

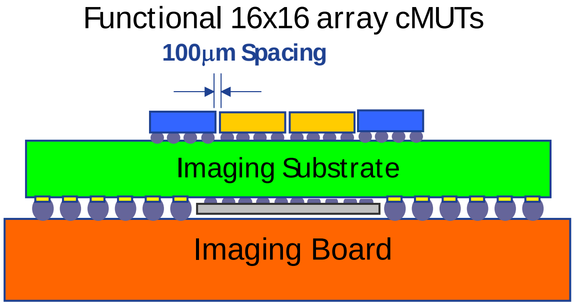


Figure 7: X-ray of cMUT attached to 1A NIP interposer showing no shorts. Note opens where cMUT pillars were missing.

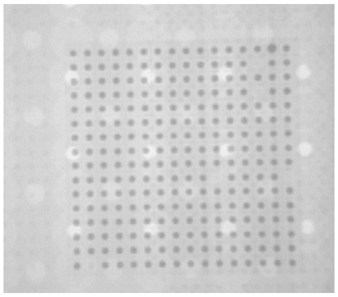


Figure 8: Photograph showing cMUT pillars detached from cMUT body after shear testing.

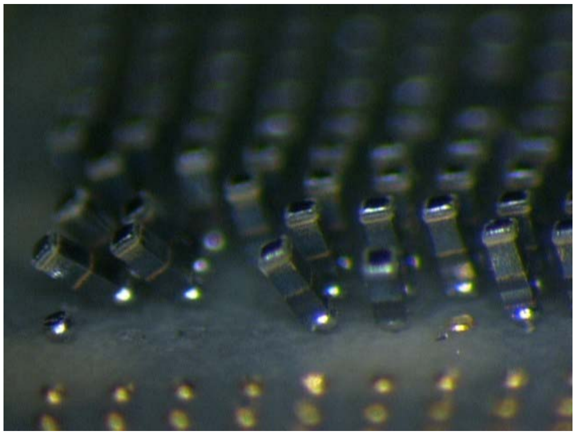


Figure 9: Photograph showing body of cMUT device after pillars were detached after shear testing.